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DATE: Wednesday, January 19, 2005

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L12	(deep adj sleep) with (output$4 near3 data)	2
☐	L11	(deep adj sleep) same (operat$4 near3 (peripheral or subsystem))	1
☐	L10	(deep adj sleep) with (operat$4 near3 (peripheral or subsystem))	0
☐	L9	(deep adj sleep) with (run$4 near3 subsystem)	1
☐	L8	l4 same l5 same l6	15
☐	L7	l4 and l5 and l6	18
☐	L6	(second adj power adj (mode or state))	126
☐	L5	(third adj power adj (mode or state))	22
☐	L4	(first adj power adj (mode or state))	113
☐	L3	L2 same process$4	53
☐	L2	L1 same power$4	130
☐	L1	(deep adj sleep)	493

END OF SEARCH HISTORY

L8: Entry 2 of 15 File: USPT Oct 5, 2004

DOCUMENT-IDENTIFIER: US 6801196 B1
TITLE: Method and apparatus to control power state of a display device

CLAIMS:

1. A method comprising: transitioning a display device from a first power state to a second power state in response to signal activity to the display device falling below a predetermined activity threshold, the second power state to consume less power than the first power state; when in the second power state, transitioning the display device to a third power state in response to the signal activity to the display device remaining below the predetermined threshold for a predetermined period of time, the third power state is to consume less power than the second power state; when in the second or third power state, transitioning the display device to the first power state in response to signal activity to the display device rising above the predetermined threshold; and when in the first, second, or third power state, transitioning the display device to a fourth power state in response to a a power control signal from a computer system separate from the monitor, the power control signal does not transition a power state of the computer system, the fourth power state is to consume less power than the third reduced power state.

5. A computer-readable medium, having stored thereon a set of instruction, the instruction when executed, perform a method comprising: transitioning a display device from a first power state to a second power state in response to signal activity to the display device falling below a predetermined activity threshold, the second power state to consume less power than the first power state; when in the second power state, transitioning the display device to a third power state in response to the signal activity to the display device remaining below the predetermined threshold for a predetermined period of time, the third power state is to consume less power than the second power state; when in the second or third power state, transitioning the display device to the first power state in response to signal activity to the display device rising above the predetermined threshold; and when in the first, second, or third power state, transitioning the display device to a fourth power state in response to a power control signal from a computer system separate from the monitor, the power control signal does not transition a power state of the computer system, the fourth power state is to consume less power than the third reduced power state.

9. An apparatus comprising: a unit to transition a display device from a first power state to a second power state in response to signal activity to the display device falling below a predetermined activity threshold, the second power state to consume less power than the first power state; when in the second power state, a unit to transition the display device to a third power state in response to the signal activity to the display device remaining below the predetermined threshold for a predetermined period of time, the third power state is to consume less power than the second power state; when in the second or third power state, a unit to transition the display device to the first power state in response to signal activity to the display device rising above the predetermined threshold; and when in the first, second, or third power state, a unit to transition the display device to a fourth power state in response to a power control signal from a computer

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		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L6	((audio or video or (real adj time)) near2 subsystem) same (process$4 near3 (power$4 near2 (mode or state)))	1
☐	L5	((audio or video or (real adj time)) near2 subsystem) same (processor$4 near3 (power$4 near2 (mode or state)))	1
☐	L4	((audio or video or (real adj time)) near2 subsystem) same (power$4 near2 (mode or state))	22
☐	L3	((audio or video or (real adj time)) near2 subsystem) same power$4	264
☐	L2	((audio or video or (real adj time)) near2 subsystem) same (deep adj sleep)	1
☐	L1	((audio or video or (real adj time)) near2 subsystem) with (deep adj sleep)	0

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L11: Entry 1 of 1 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665802 B1
** See image for Certificate of Correction **
TITLE: Power management and control for a microcontroller

Detailed Description Text (37):
The sleep mode (clock distributed mode) is a subset of the sleep mode and it can include sleep with clocks, no clocks and deep sleep where power may be disabled. In this mode, the PLL and oscillator are not stopped and the clock is distributed to the system. The sleep mode may be entered under program control when substantial power saving is desired and a quick response to interrupt events is required or background functionality is required. This mode allows the operating system to stop the clock for CPU 22 and selected peripheral clocks to reduce power consumption while waiting for internal or external interrupt events. This mode also allows the option of operating only those peripherals having a reduced clock frequency. When an interrupt is detected, all systems begin clocking and execution starts. During this sleep mode with clock distributed, all other on-chip clocks, PLL's and devices not explicitly stopped by program control function normally. As mentioned above, the response to the subsystems 30 through 40 to the various power modes are configured under program control. Thus, the peripheral interface control register may be set during a supervisory mode of the CPU core 22 which will enable seep ES and divide clock bits. The CPU core may configure any reduced speed through the power management state machine configuration register bits 19:16 by configuring the clock source CLKSRC bits and the sleep clock bits 26:24.

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Hide?	Set Name	Query	Hit Count
	DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L4	(power$4 near2 (mode or state)) with (processor or (processing adj (unit or circuit))) with (output$4 near3 data)	19
☐	L3	(output$4 near3 (audio or video or multimedia)) near5 ((power$4 near2 down) or sleep)	23
☐	L2	(output$4 near3 (audio or video or multimedia)) with ((power$4 near2 down) or sleep)	64
☐	L1	(audio or video) with (upload$4 or download$4) with ((power$4 near2 down) or sleep)	2

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L3: Entry 5 of 23 File: USPT Nov 13, 2001

DOCUMENT-IDENTIFIER: US 6316993 B1
TITLE: Analog circuitry for start-up glitch suppression

Brief Summary Text (4):
Standard audio output drivers are capacitively coupled, or at least have bypass capacitors, to ground. Thus, if an operational amplifier (op amp) which drives the audio output is powered down during a "sleep" mode, for example, to save system power, the capacitor at the output will experience a small charge as the op amp is powered down, or a small discharge when the op amp is powered up. This charging and discharging will cause the voltage to change, and will be heard through the speaker load. The sound is like a "pop" or a "click", and is considered to be highly undesirable in audio systems.

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L3: Entry 1 of 23 File: USPT Apr 6, 2004

DOCUMENT-IDENTIFIER: US 6715673 B2
TITLE: Automated fee collection and parking ticket dispensing machine

Detailed Description Text (76):
When the machine 2 is otherwise in sleep mode, the audio and visual output capabilities of the machine 2 may be used to present advertising or other information. The presentation of such information may be interrupted when a user pushes a display button. The audio and visual output capabilities may also be used to present information to a user regarding available transactions. For example, an embodiment of the machine 2 having a "theater" operational mode adapted for placement in a mall or theater may present information regarding upcoming film showings, indicating time and cost, and may even offer clips or "trailers" of selected films. A user could then purchase tickets to the desired show. Upon issuing the purchased tickets, the machine 2 could then present coupons, either preprinted or printed upon issuance, to the user for refreshments at the theater or for goods or services available from nearby establishments.

L3: Entry 8 of 23 File: USPT Nov 14, 2000

DOCUMENT-IDENTIFIER: US 6148345 A
TITLE: Power savings for sound system

CLAIMS:

1. A computer system comprising:

a sound controller for controlling reproduction of sound data, wherein said sound controller comprises sound reproduction means for converting sound data transferred from a memory of said computer system via DMA transfer to said sound controller into an audio signal, and means for externally outputting a second power down signal for setting an analog audio circuit serving as a peripheral circuit of said sound controller to receive an analog audio signal in a power down mode when a first power down signal is received;

a DMA controller having means for generating the first power down signal based on end timing of the DMA transfer for transferring the sound data and means for transferring sound data to be reproduced from the memory of said computer system to said sound controller using the DMA transfer; and

a power supply circuit for supplying electric power to said analog audio circuit, said power supply circuit switching supply of the electric power to said analog audio circuit in accordance with the second power down signal output from said means for externally outputting,

wherein said sound controller comprises a copy register in which a copy of a register value set in the DMA controller of said computer system for the purpose of the DMA transfer of the sound data is written, and said means for generating the second power down signal detects the end timing of the DMA transfer for transferring the sound data in response to a write of the copy of the register value in the DMA controller to said copy register, and a transfer completion signal from the DMA controller.